REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 106, 110, 112-114, 120, 136, 141-145, 153 and 155 are pending; Claims 106, 110, 112-114, 120, 136, 141-145, 153 and 155 have been currently amended; Claims 1-105, 107-109, 111, 115-119, 121-135, 137-140, 146-152 and 154 have been canceled. No new matter is believed to be added.

Response to Claim Rejections under 35 U.S.C. 112, first paragraph

Reconsideration of Claims 120, 123, 126-129, 136, 139, 140, 143-153 and 155 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement is requested based on amended Claims 120 and 136 and on the following remarks.

Figs. 12a-12h shows a method for transitioning from a fine-line interconnection to the post passivation interconnection of the invention, and one method for forming the post passivation interconnection. *~ See the sixth paragraph on page 8, in the original specification ~*

Fig. 7 shows a post-passivation structure (over a passivation layer) for a solder bump or wirebonding. *~ See lines 13-15 on page 26, in the original specification ~*

Based on the disclosure, the process of Figs. 12a-12g can be applied to forming the post passivation structure of Fig. 7. After the post-passivation structure is formed based on the process of Figs. 12a-12g, a wirebond can be formed on the post-passivation structure.

Response to Claim Rejections under 35 U.S.C. 102 and 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 106, 110, 112-114, 119, 141 and 142

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As currently amended, independent Claim 106 is recited below:

106. A semiconductor chip connected to a wirebond interconnect, comprising:

a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein a first opening in said passivation layer is over said first region and exposes said first region, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;

a polymer layer on said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness between 2 and 50 μm and greater than that of said passivation layer; and

a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises an electroplated gold layer with a thickness between 2 and 100 μm, wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different.

Reconsiderations of Claims 106-110, 112, 113, 116, 119, 141 and 142 rejected under 35 U.S.C. 102(e) as being anticipated by Leu et al. (U.S. Pat. No. 6,605,549) and of Claims 114, 115 and 154 rejected under 35 U.S.C. 103(a) as being unpatentable over Leu et al. in view of Kikuchi (U.S. Pub. No. 2003/0102551) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip connected to a wirebond interconnect, as claimed in amended Claim 106, patentably distinguishes over the citation by Leu et al. (U.S. Pat. No. 6,605,549).

Leu et al. teach a damascene process including forming a barrier layer 45 in openings 49A, 49B and 48 in a dielectric layer 42, forming a seed layer 50 on the barrier layer 45, forming a metal layer 52 on the seed layer 50 and removing the metal layer 52, seed layer 50 and barrier layer 45 outside the openings 49A, 49B and 48 by a chemical-mechanical polishing (CMP) process. ~ *See Figs. 4A-4E; col. 8, lines 49-60; col. 9, lines 25-28; col. 10, lines 5-10 and 40-47* ~

The Examiner considers that the reference number of 55 can be deemed as the claimed passivation layer. ~ *See line 6 in point 4, on page 3, in the last Office Action mailed Jul. 19, 2007* ~

Applicants respectfully traverse the Examiner's opinions because Leu et al. fail to teach the dielectric layer 55 may comprise an oxide layer and a nitride layer over said oxide layer, which composes necessary elements of the claimed passivation layer as claimed in Claim 106.

Leu et al. teach the dielectric layer 55 is not on a top surface of a pad. However, applicants teach there may be a passivation layer on a second region of a top surface of a contact pad, and an opening in the passivation layer is over a first region of the top surface of the contact pad and exposes the first region, as claimed in Claim 106 and not taught by Leu et al.

Furthermore, Leu et al. fail to teach a second contact pad connected to a wirebond interconnect may have a different position from that of a first contact pad exposed by an opening in a passivation layer, as claimed in Claim 106.

Besides, applicants find gold is soft and well compliant with absorbing an impact from an external force. Therefore, applicants try to form a wirebonding pad with a thick electroplated gold layer having a thickness greater than 2 micrometers, as claimed in Claim 106, for being connected with a wire formed by a wirebonding process and find it works. It is believed that one skilled in the art can not anticipate the claimed wirebonding pad, as claimed in Claim 106, because Leu et al. fail to teach the above-mentioned motivation.

For at least the foregoing reasons, withdrawal of rejection under 35 U.S.C. 102(e) to Claim 106 is respectfully requested.

Applicants respectfully submit independent Claim 106 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 110, 112-114, 119, 141 and 142 patently define over the prior art as well.

Response to Claims 120, 129, 143-145 and 155

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As previously presented, independent Claim 120 is recited below:

120. A semiconductor chip connected to a wirebond interconnect, comprising:
a silicon substrate;
a transistor in or on said silicon substrate;
a metallization structure over said silicon substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;
a dielectric layer between said first and second metal layers;
a first contact pad over said silicon substrate;
a passivation layer over said metallization structure and over said dielectric layer, wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;
a polymer layer on said passivation layer, wherein an opening in said polymer layer is over said first contact pad and exposes said first contact pad, and wherein said polymer layer has a thickness between 2 and 50 μm and greater than that of said passivation layer; and
a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises an electroplated gold layer with a thickness between 2 and 100 μm, wherein said second contact pad is connected to said first contact pad through said opening, and wherein the positions of said first and second contact pads from a top perspective view are different.

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Reconsiderations of Claims 120, 123, 126-129 and 131 rejected under 35 U.S.C. 102(e) as being anticipated by or under 35 U.S.C. 103(a) as being obvious over Kikuchi (U.S. Pub. No. 2003/0102551) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip connected to a wirebond interconnect, as claimed in amended Claim 120, patentably distinguishes over the citation by Kikuchi (U.S. Pub. No. 2003/0102551).

The Examiner considers that the reference number of 130 can be deemed as the claimed passivation layer. *~ See lines 6 and 7 in point 5, on pages 5 and 6, in the last Office Action mailed Jul. 19, 2007 ~*

Applicants respectfully traverse the Examiner's opinions. Kikuchi teaches the element 130 is a protective layer formed using silicon oxide or silicon nitride. *~ See lines 6 and 7, in par. [0039] ~* However, Kikuchi fails to teach the protective layer 130 may comprise an oxide layer and a nitride layer over the oxide layer, as defined by the claimed passivation layer, as claimed in Claim 120.

Kikuchi teaches that there may be a thin polymer layer 140 with a thickness of 1 μm on a passivation layer. *~ See lines 8-11, in par. [0040] ~* However, Kikuchi fails to teach there may be thick polymer layer with a thickness between 2 and 50 μm, as claimed in Claim 120, on a passivation layer. The thick polymer layer can prevent the underlying devices from being damaged by an undesired force because the thick polymer layer is soft and well compliant with absorbing an impact from the undesired force. It is believed that one skilled in the art can not anticipate the claimed thick polymer layer, as claimed in Claim 120, because Kikuchi fails to teach the above-mentioned motivation.

Furthermore, Kikuchi fails to teach a second contact pad connected to a wirebond interconnect may have a different position from that of a first contact pad exposed by an opening in a passivation layer, as claimed in Claim 120.

Besides, applicants find gold is soft and well compliant with absorbing an impact from an external force. Therefore, applicants try to form a wirebonding pad with a thick electroplated gold layer having a thickness greater than 2 micrometers, as claimed in Claim 120, for being connected with a wire formed by a wirebonding process and find it works. It is believed that one skilled in the art can not anticipate the claimed wirebonding pad, as claimed in Claim 120, because Kikuchi fails to teach the above-mentioned motivation.

For at least the foregoing reasons, withdrawal of rejection under 35 U.S.C. 102(e) and under 35 U.S.C. 103(a) to Claim 120 is respectfully requested.

Applicants respectfully submit independent Claim 120 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 129, 143-145 and 155 patently define over the prior art as well.

Response to Claims 136, 140 and 153

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As currently amended, independent Claim 136 is recited below:

136. A semiconductor chip connected to a wirebond interconnect, comprising:
a silicon substrate;

a transistor in or on said silicon substrate;

a metallization structure over said semiconductor substrate, wherein said metallization structure comprises a first metal layer and a second metal layer over said first metal layer;

a dielectric layer between said first and second metal layers;

a first contact pad over said silicon substrate, wherein said first contact pad has a top surface with a first region and a second region, wherein said second region surrounds said first region;

a passivation layer over said metallization structure, over said dielectric layer and on said second region, wherein a first opening in said passivation layer is over said first region and exposes said first region, and wherein said passivation layer comprises an oxide layer and a nitride layer over said oxide layer;

a polymer layer on said passivation layer, wherein a second opening in said polymer layer is over said first region and exposes said first region, and wherein said polymer layer has a thickness between 2 and 50 μm and greater than that of said passivation layer; and

a second contact pad connected to said wirebond interconnect, wherein said second contact pad comprises a titanium-containing layer with a thickness between 0.01 and 3 μm, a seed layer with a thickness between 0.05 and 3 μm over said titanium-containing layer, and an electroplated gold layer with a thickness between 2 and 100 μm on said seed layer, wherein said second contact pad is connected to said first contact pad through said first and second openings, and wherein the positions of said first and second contact pads from a top perspective view are different.

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Section I:

Reconsiderations of Claim 136 rejected under 35 U.S.C. 102(e) as being anticipated by Leu et al. (U.S. Pat. No. 6,605,549) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip connected to a wirebond interconnect, as claimed in amended Claim 136, patentably distinguishes over the citation by Leu et al. (U.S. Pat. No. 6,605,549).

Leu et al. teach a damascene process including forming a barrier layer 45 in openings 49A, 49B and 48 in a dielectric layer 42, forming a seed layer 50 on the barrier layer 45, forming a metal layer 52 on the seed layer 50 and removing the metal layer 52, seed layer 50 and barrier layer 45 outside the openings 49A, 49B and 48 by a chemical-mechanical polishing (CMP) process. ~ *See Figs. 4A-4E; col. 8, lines 49-60; col. 9, lines 25-28; col. 10, lines 5-10 and 40-47* ~

The Examiner considers that the reference number of 55 can be deemed as the claimed passivation layer. ~ *See line 6 on page 5, in the last Office Action mailed Jul. 19, 2007* ~

Applicants respectfully traverse the Examiner's opinions because Leu et al. fail to teach the dielectric layer 55 may comprise an oxide layer and a nitride layer over said oxide layer, which compose necessary elements of the claimed passivation layer as claimed in Claim 136.

Leu et al. teach the dielectric layer 55 is not on a top surface of a pad. However, applicants teach there may be a passivation layer on a second region of a top surface of a contact pad, and an opening in the passivation layer is over a first region of the top surface of the contact pad and exposes the first region, as claimed in Claim 136 and not taught by Leu et al.

Furthermore, Leu et al. fail to teach a second contact pad connected to a wirebond interconnect may have a different position from that of a first contact pad exposed by an opening in a passivation layer, as claimed in Claim 136.

Besides, applicants find gold is soft and well compliant with absorbing an impact from an external force. Therefore, applicants try to form a wirebonding pad with a thick electroplated gold layer having a thickness greater than 2 micrometers, as claimed in Claim 136, for being connected with a wire formed by a wirebonding process and find it works. It is believed that one skilled in the art can not anticipate the claimed wirebonding pad, as claimed in Claim 136, because Leu et al. fail to teach the above-mentioned motivation.

For at least the foregoing reasons, withdrawal of rejection under 35 U.S.C. 102(e) to Claim 136 is respectfully requested.

Section II:

Reconsiderations of Claims 136, 140 and 153 rejected under 35 U.S.C. 102(e) as being anticipated by or under 35 U.S.C. 103(a) as being obvious over Kikuchi (U.S. Pub. No. 2003/0102551) are requested based on the following remarks.

Applicants respectfully assert that the semiconductor chip connected to a wirebond interconnect, as claimed in amended Claim 136, patentably distinguishes over the citation by Kikuchi (U.S. Pub. No. 2003/0102551).

The Examiner considers that the reference number of 130 can be deemed as the claimed passivation layer. *~ See line 3 in the last paragraph, on page 7, in the last Office Action mailed Jul. 19, 2007 ~*

Applicants respectfully traverse the Examiner's opinions. Kikuchi teaches the element 130 is a protective layer formed using silicon oxide or silicon nitride. ~ *See lines 6 and 7, in par. [0039]* ~ However, Kikuchi fails to teach the protective layer 130 may comprise an oxide layer and a nitride layer over the oxide layer, as defined by the claimed passivation layer, as claimed in Claim 136.

Kikuchi teaches that there may be a thin polymer layer 140 with a thickness of 1 μm on a passivation layer. ~ *See lines 8-11, in par. [0040]* ~ However, Kikuchi fails to teach there may be thick polymer layer with a thickness between 2 and 50 μm, as claimed in Claim 136, on a passivation layer. The thick polymer layer can prevent the underlying devices from being damaged by an undesired force because the thick polymer layer is soft and well compliant with absorbing an impact from the undesired force. It is believed that one skilled in the art can not anticipate the claimed thick polymer layer, as claimed in Claim 136, because Kikuchi fails to teach the above-mentioned motivation.

Furthermore, Kikuchi fails to teach a second contact pad connected to a wirebond interconnect may have a different position from that of a first contact pad exposed by an opening in a passivation layer, as claimed in Claim 136.

Besides, applicants find gold is soft and well compliant with absorbing an impact from an external force. Therefore, applicants try to form a wirebonding pad with a thick electroplated gold layer having a thickness greater than 2 micrometers, as claimed in Claim 136, for being

connected with a wire formed by a wirebonding process and find it works. It is believed that one skilled in the art can not anticipate the claimed wirebonding pad, as claimed in Claim 136, because Kikuchi fails to teach the above-mentioned motivation.

For at least the foregoing reasons, withdrawal of rejection under 35 U.S.C. 102(e) and under 35 U.S.C. 103(a) to Claim 136 is respectfully requested.

Applicants respectfully submit independent Claim 136 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent Claims 140 and 153 patently define over the prior art as well.

CONCLUSION

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Le not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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